EE 508 Lecture 40

Some Recent Filter Structures

A Power-Efficient Reconfigurable OTA-C Filter for Low-Frequency Biomedical Applications

Sheng-Yu Peng, *Member, IEEE*, Yu-Hsien Lee, Tzu-Yun Wang, *Student Member, IEEE*, Hui-Chun Huang, Min-Rui Lai, Chiang-Hsi Lee, and Li-Han Liu

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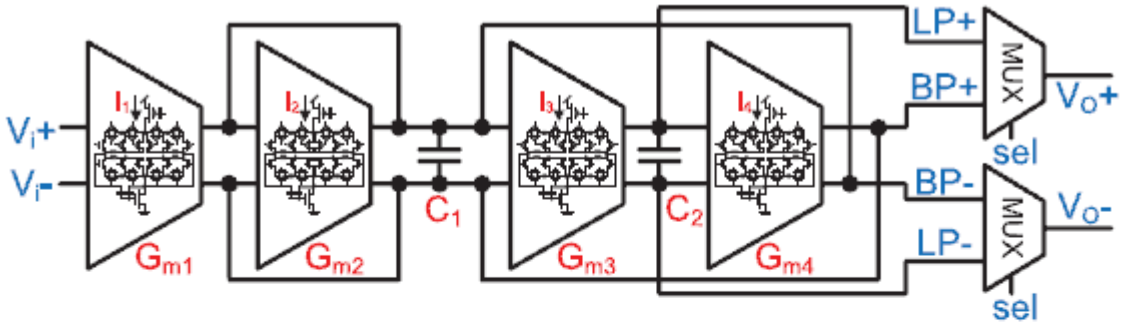
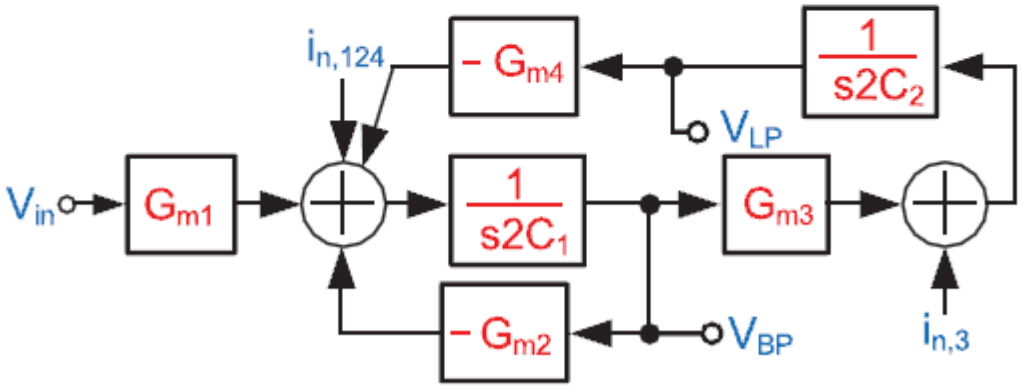
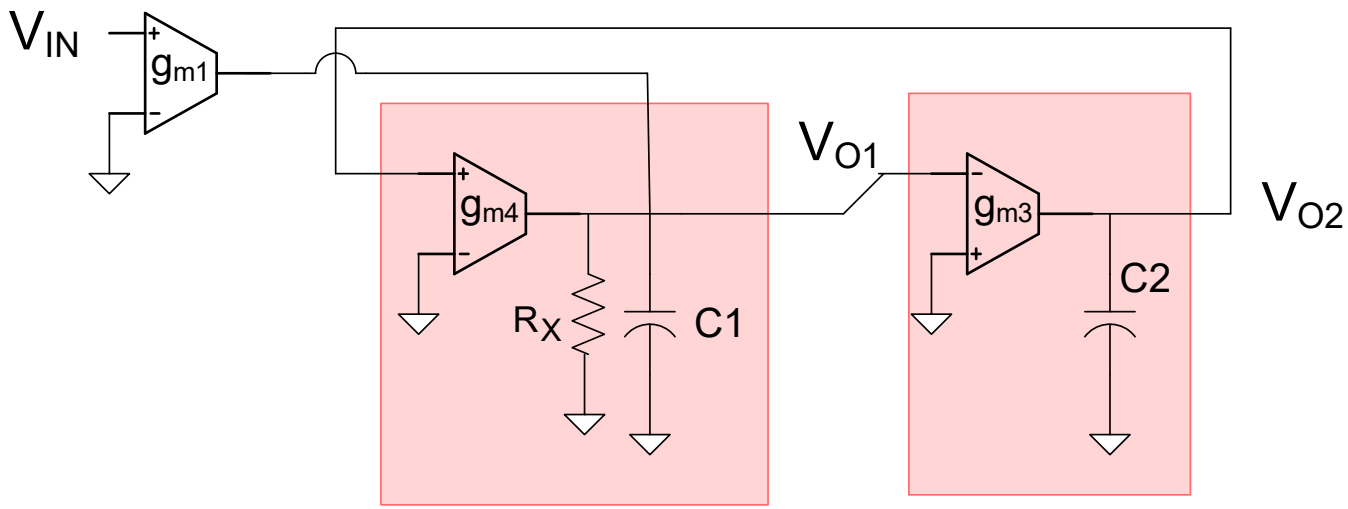


(a)



(b)

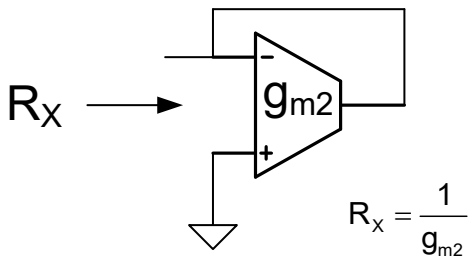
Recall the basic two-integrator loop



$$\left.\begin{aligned} V_{01}sC_1 &= G_X V_{01} + g_{m1}V_{IN} + g_{m4}V_{02} \\ V_{02}sC_2 &= g_{m3}V_{01} \end{aligned}\right\}$$

$$\frac{V_{01}}{V_{IN}} = \frac{s\dfrac{g_{m1}}{C_1}}{s^2 + s\dfrac{g_X}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$

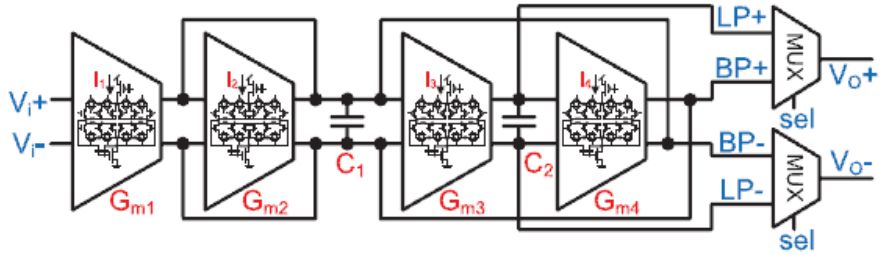
$$\frac{V_{02}}{V_{IN}} = \frac{\dfrac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\dfrac{g_X}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$



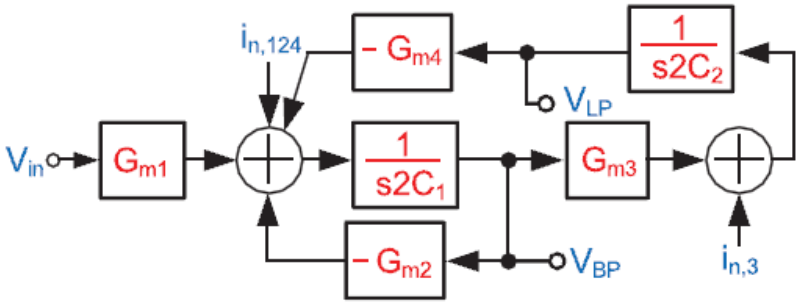
$$R_X = \frac{1}{g_{m2}}$$

$$\frac{V_{01}}{V_{IN}} = \frac{s\dfrac{g_{m1}}{C_1}}{s^2 + s\dfrac{g_{m2}}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$

$$\frac{V_{02}}{V_{IN}} = \frac{\dfrac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\dfrac{g_{m2}}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$



(a)

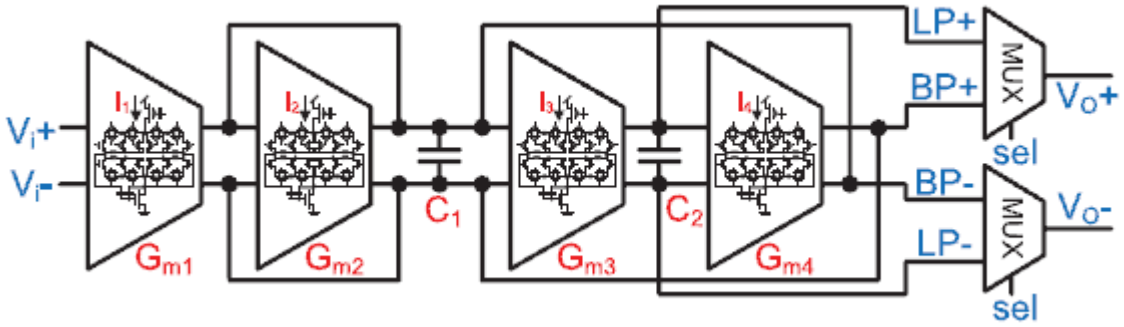


(b)

- This is a fully-differential implementation of the standard two-integrator loop
- MUX selects either LP or BP output

$$\frac{V_{01}}{V_{IN}} = \frac{s\frac{g_{m1}}{C_1}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}$$

$$\frac{V_{02}}{V_{IN}} = \frac{\frac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}$$



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OTAs operate in weak inversion

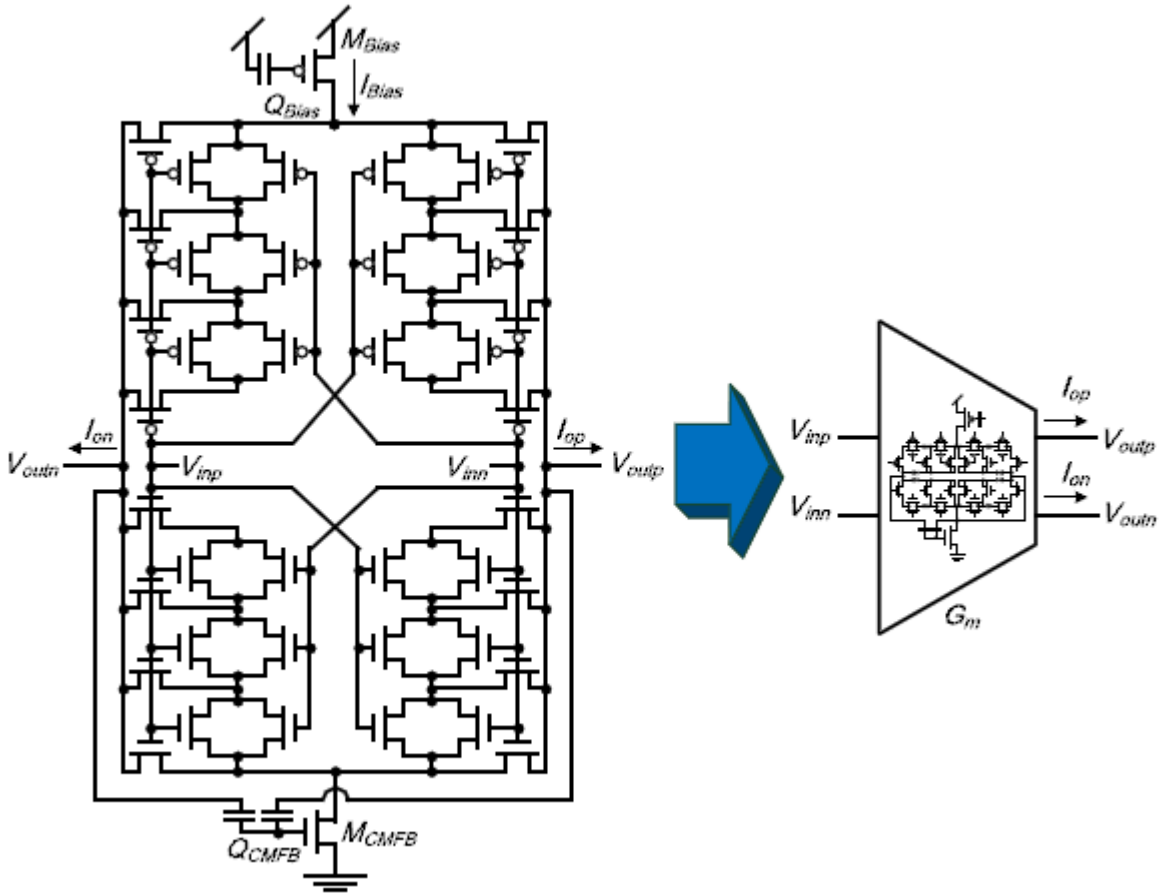
Adjust ω0 by changing tail currents – claim in excess of 5 decades of adjustment

Target 2Hz to 20KHz though claim can go much lower (claim to 10mHz range) and higher

Bias current adjusted by changing charge on floating gate transistor

Each biquad requires 0.12mm^2 of die area in 350nm process

Linearized OTA

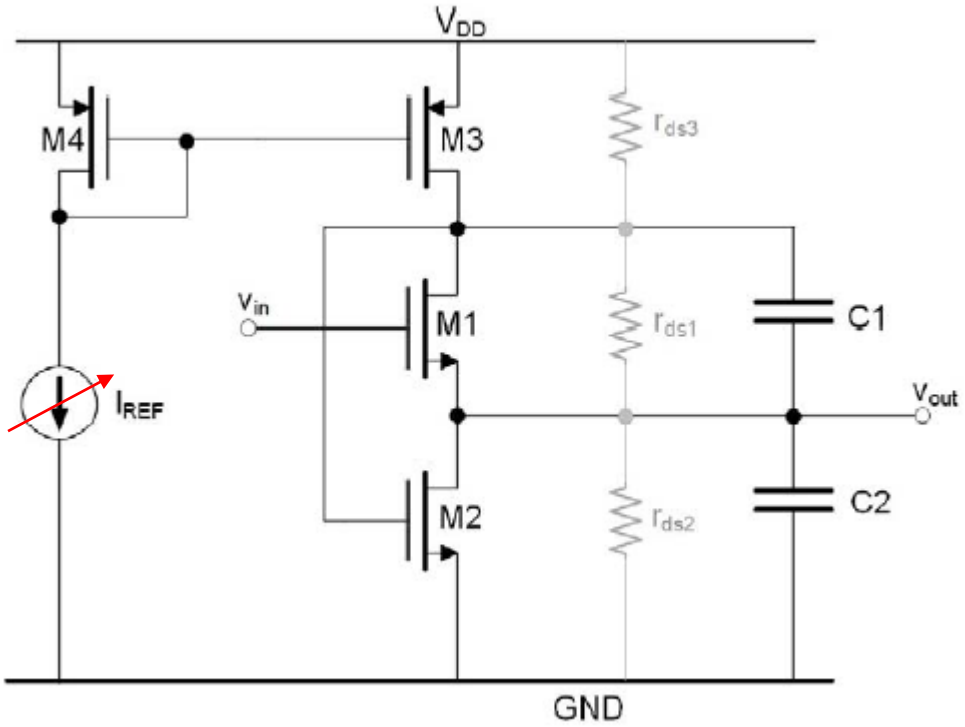


Used computer iteration to size devices in OTA
Good linearity and low power dissipation claimed

A 28nm-CMOS 100MHz 1mW 12dBm-IIP3 4th-order Flipped-Source-Follower Analog Filter

F. Fary1, M. De Matteis1, T. Vergine1,2 and A. Baschirotto1

ESSCIRC 2018

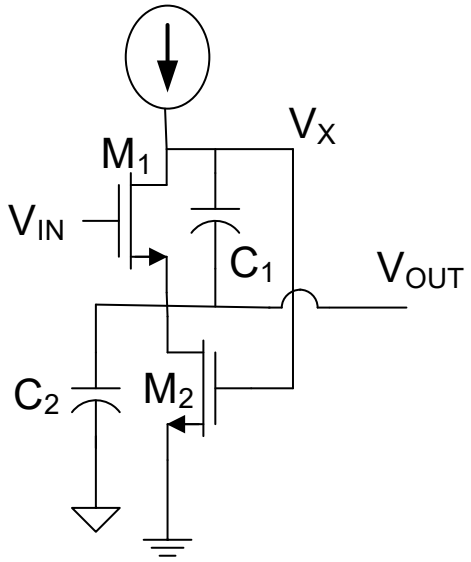


Flipped-Source-Follower NMOS Biquadratic Cell

Table 1 – Filter Design Paramters

Transfer Function		*4th-Order Low-Pass*	
dc-Gain		0dB	
Poles Frequency		100 MHz	
Cell A Q Factor	1.306	**Cell B Q Factor**	0.5412
Cell A g_{m1}- g_{m2}	1.8 mA/V	**Cell B g_{m1}- g_{m3}**	1.8 mA/V
Cell A - C_{1a}	4.8 pF	**Cell B - C_{1b}**	1.99 pF
Cell A - C_{2a}	1.75 pF	**Cell B - C_{2b}**	3.98 pF

A=0.026mm^2 for 4th order BW filter in 28nm process P approx. 1mW



$$\left.\begin{aligned} &V_{OUT}\left(sC_1+sC_2\right)+g_{m2}V_{GS2}-g_{m1}V_{GS1}=sC_1V_{GS2}\\ &V_{IN}=V_{GS1}+V_{OUT}\\ &V_{GS2}sC_1+g_{m1}V_{GS1}=V_{OUT}sC_1 \end{aligned}\right\}$$

$$\frac{V_{OUT}}{V_{IN}}=\frac{g_{m1}g_{m2}}{s^2C_1C_2+sC_1g_{m2}+g_{m1}g_{m2}}$$

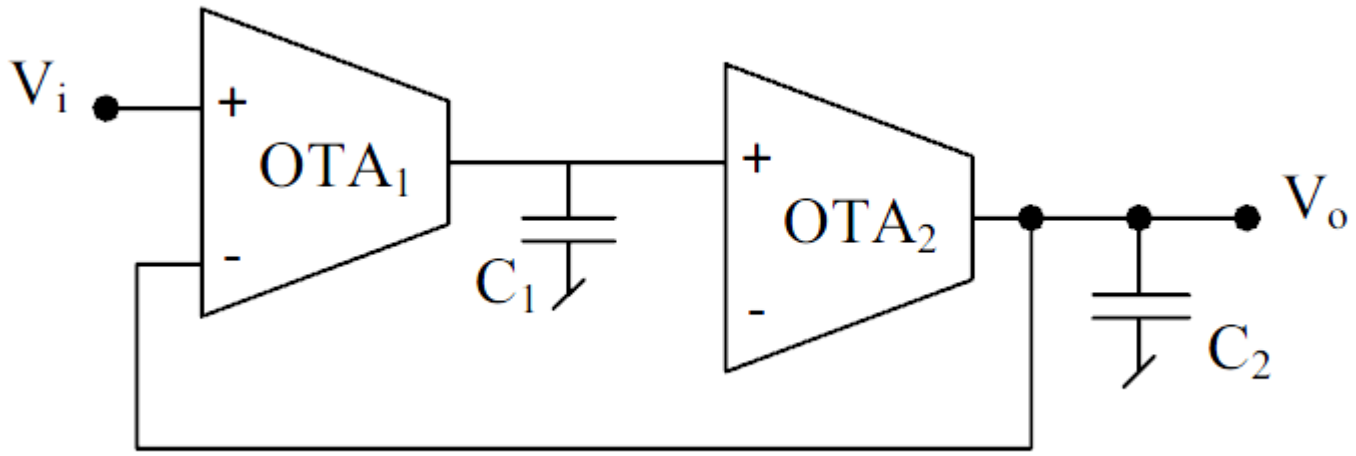
$$\omega_0=\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$Q=\sqrt{\frac{g_{m1}}{g_{\partial m2}}\frac{C_2}{C_1}}$$

A New Method to Design Multi-Standard Analog Baseband Low-Pass Filter

Ersin Alaybeyoğlu[1], Hakan Kuntman[2]

2017 10th International Conference on Electrical and Electronics Engineering (ELECO)



$$\frac{V_{LP}}{V_{in}} = \frac{g_{m1}g_{m2}}{s^2C_1C_2 + sC_1g_{m1} + g_{m1}g_{m2}}$$

$$w_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$Q = \sqrt{\frac{C_2g_{m2}}{C_1g_{m1}}}$$

10MHz – 40MHz

Projected Area 0.02mm^2 in 180nm proc

Low-Power *Gm–C* Filter Employing Current-Reuse Differential Difference Amplifiers

John S. Mincey, *Student Member, IEEE*, Carlos Briseno-Vidrios, *Student Member, IEEE*,
Jose Silva-Martinez, *Fellow, IEEE*, and Christopher T. Rodenbeck, *Senior Member, IEEE*

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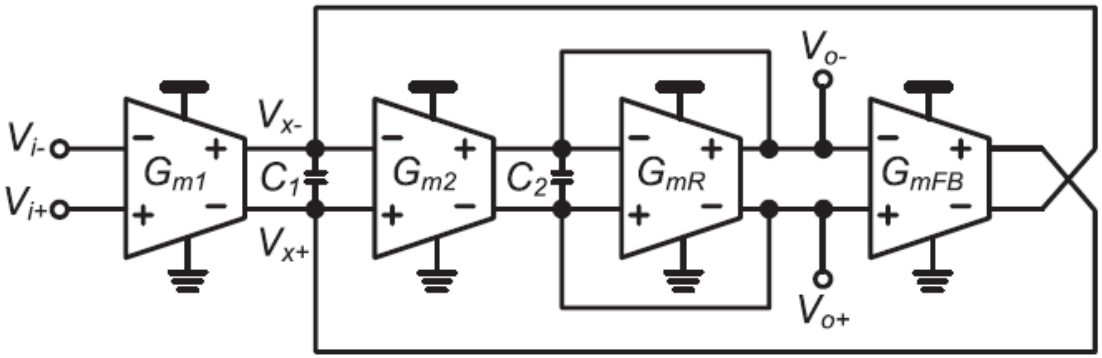
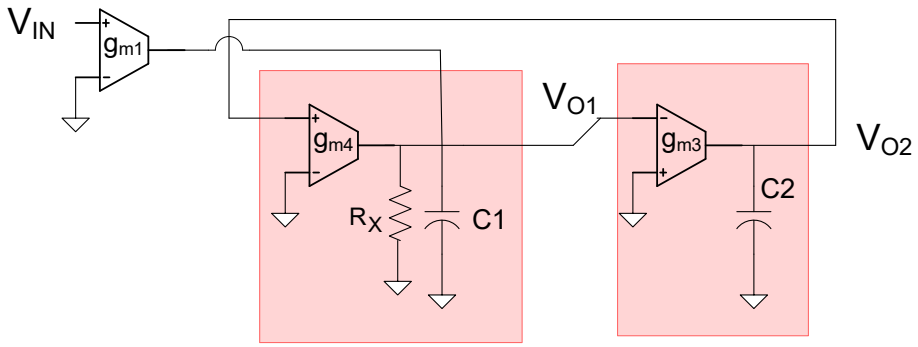
Typical Differential Implementation



Typical Single-Ended Implementation



Require 4 OTAs

Current-reuse Structures

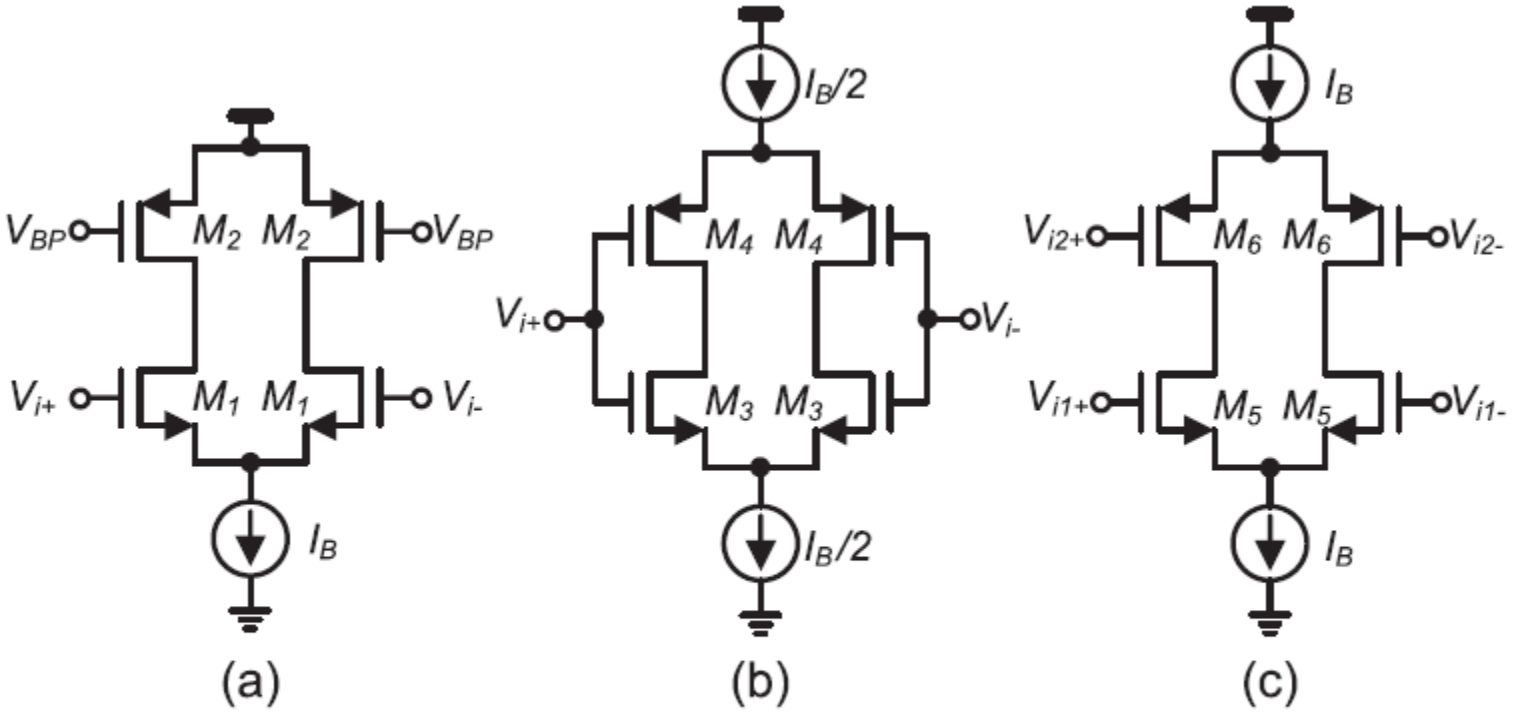


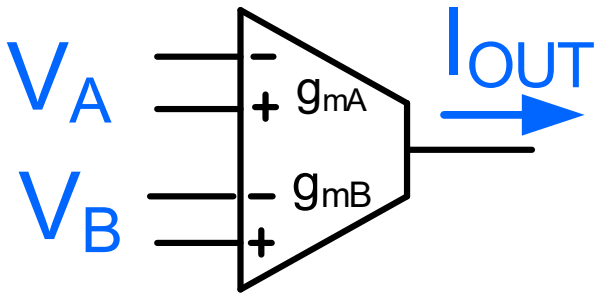
Fig. 3. (a) Conventional differential pair. (b) DDP using half the bias current. (c) Current-reuse DDA.

Dual Differential Pair: DDP

Dual Different Amplifier: DDA

Current Reuse offers potential for significant power reduction

Current-reuse Structures

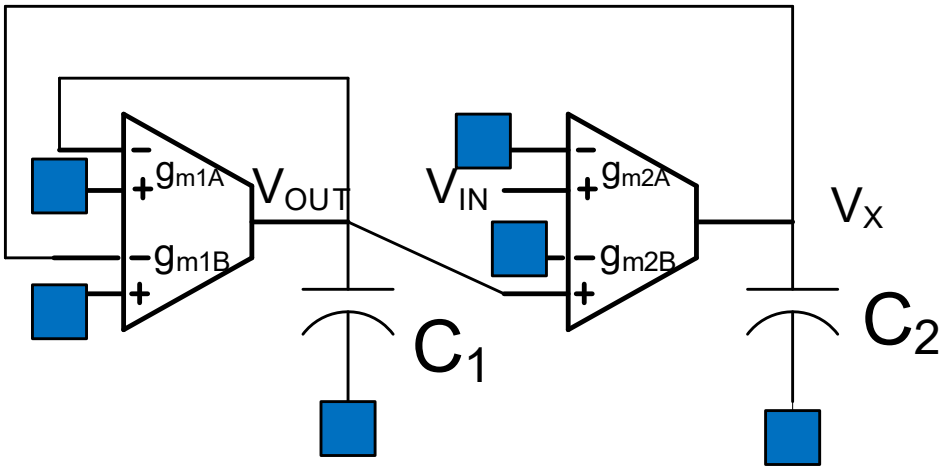


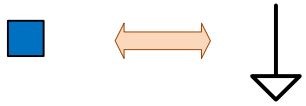
Dual input OTA

$$I_{OUT} = g_{mA} V_A + g_{mB} V_B$$

Current-reuse Structures

Consider:





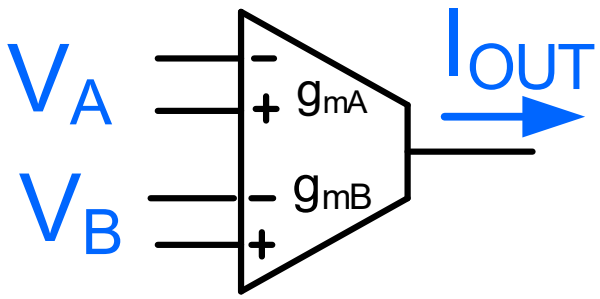
$$\left.\begin{aligned} V_{OUT}sC_1 &= -g_{m1A}V_{OUT} + g_{m1B}V_X \\ V_X sC_2 &= g_{m2B}V_{OUT} + g_{m2A}V_{IN} \end{aligned}\right\}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{g_{m2A}g_{m1B}}{\left(s^2C_1C_2 + sC_2g_{m1A} + g_{m1B}g_{m2B}\right)}$$

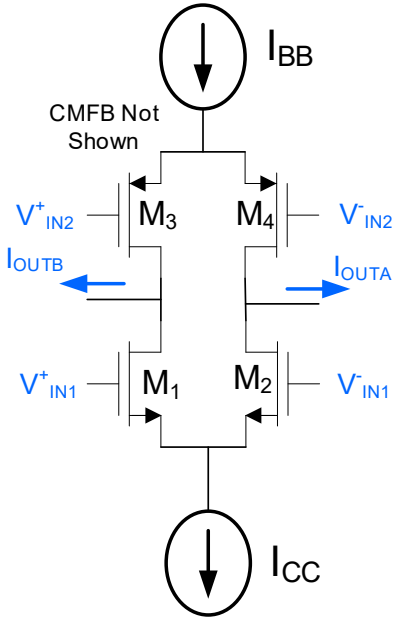
Realizes 2nd-order lowpass with just 2 OTAs

Current-reuse Structures

Dual input OTA



$$I_{OUT} = g_{mA} V_A + g_{mB} V_B$$

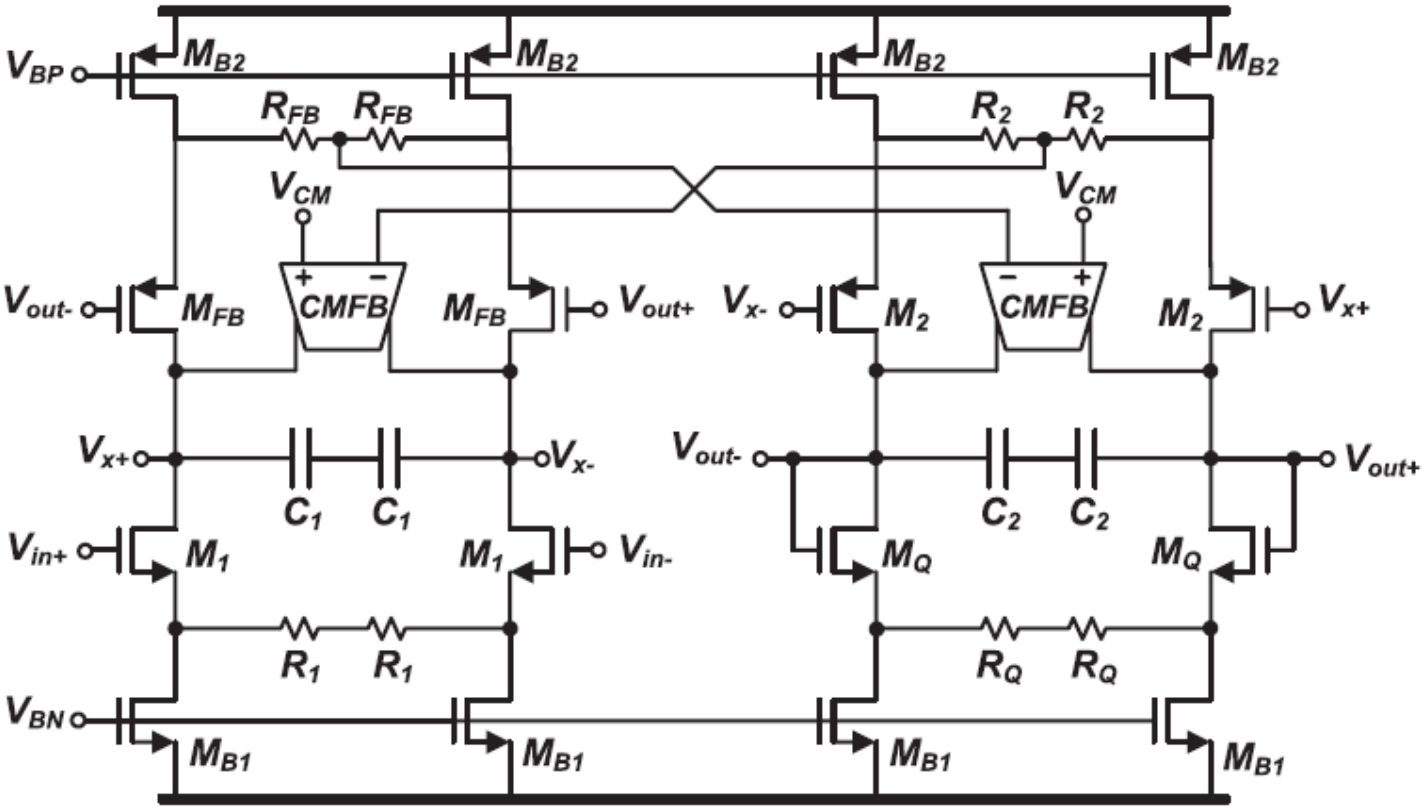


$$I_{OUTA} = g_{m2} V^-_{IN1} + g_{m4} V^-_{IN2}$$

$$I_{OUTB} = g_{m1} V^+_{IN1} + g_{m3} V^+_{IN2}$$

Current-reuse Structures

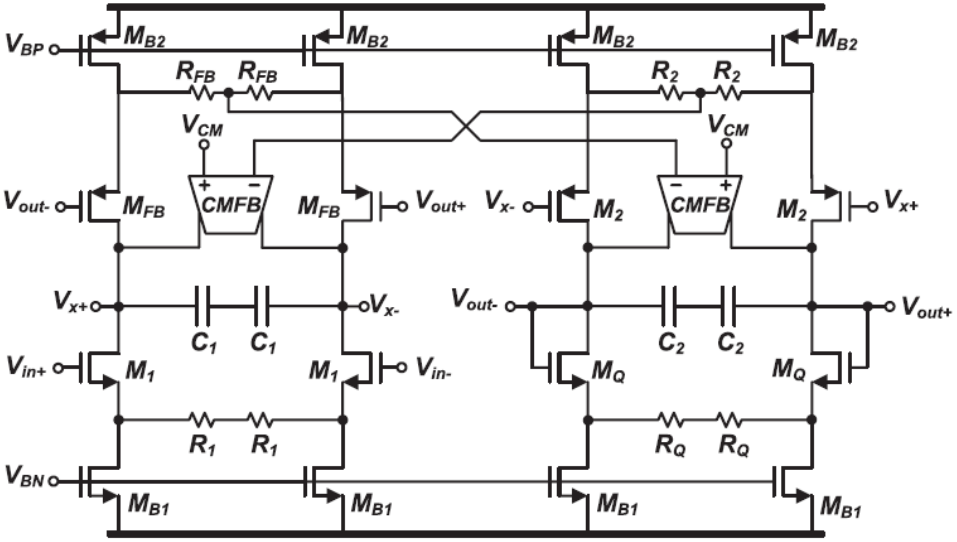
Dual input OTA



2nd Order Lowpass Biquad using Current-reuse OTA

Current-reuse Structures

Dual input OTA



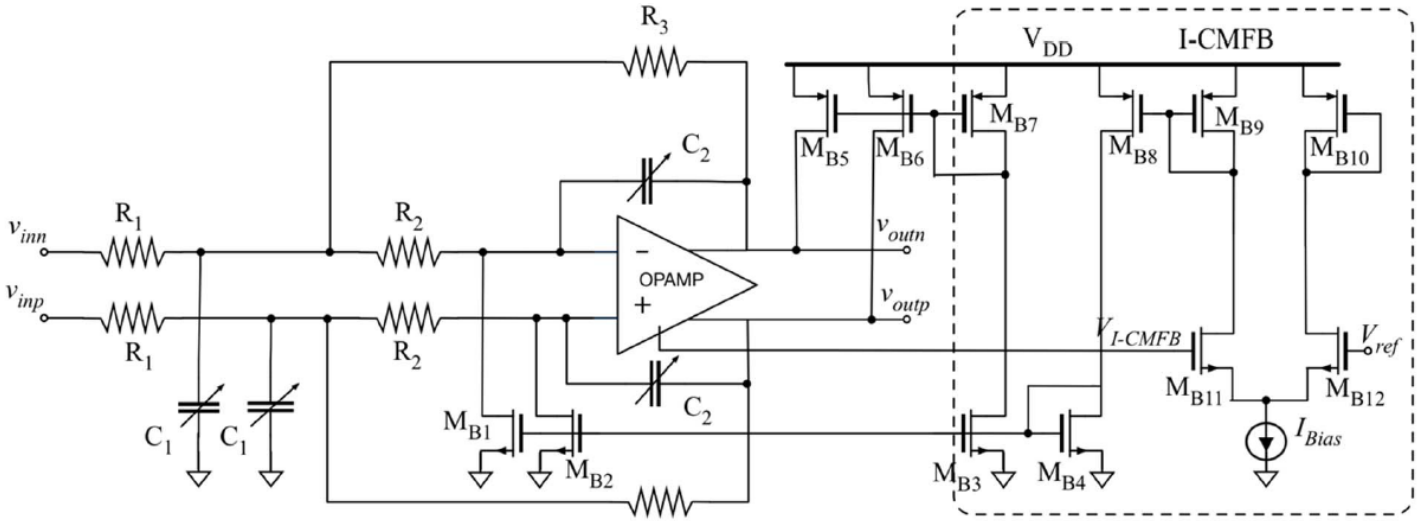
Sixth-order Butterworth G_m–C filter was fabricated

- 180-nm CMOS process
- total chip area of 0.21 mm^2
- 65MHz Band Edge
- 1.3mW/pole

A 0.9V 75MHz 2.8mW 4th-Order Analog Filter in CMOS-Bulk 28nm Technology

F. Ciciotti, M. De Matteis, and A. Baschirotto

ISCAS 2018



$$H(s) \cong -\frac{R_3}{R_1} \cdot \frac{1}{1 + sC_2\left(R_2 + R_3 + R_2\frac{R_3}{R_1}\right) + s^2 C_1 C_2 R_2 R_3}$$

$$\omega_0 = \sqrt{\frac{1}{R_2 R_3 C_1 C_2}} \qquad Q = \sqrt{\frac{C_1}{C_2}} \frac{\sqrt{R_2 R_3}}{R_2 + R_3 + \frac{R_2 R_3}{R_1}}$$

A 0.9V 75MHz 2.8mW 4th-Order Analog Filter in CMOS-Bulk 28nm Technology

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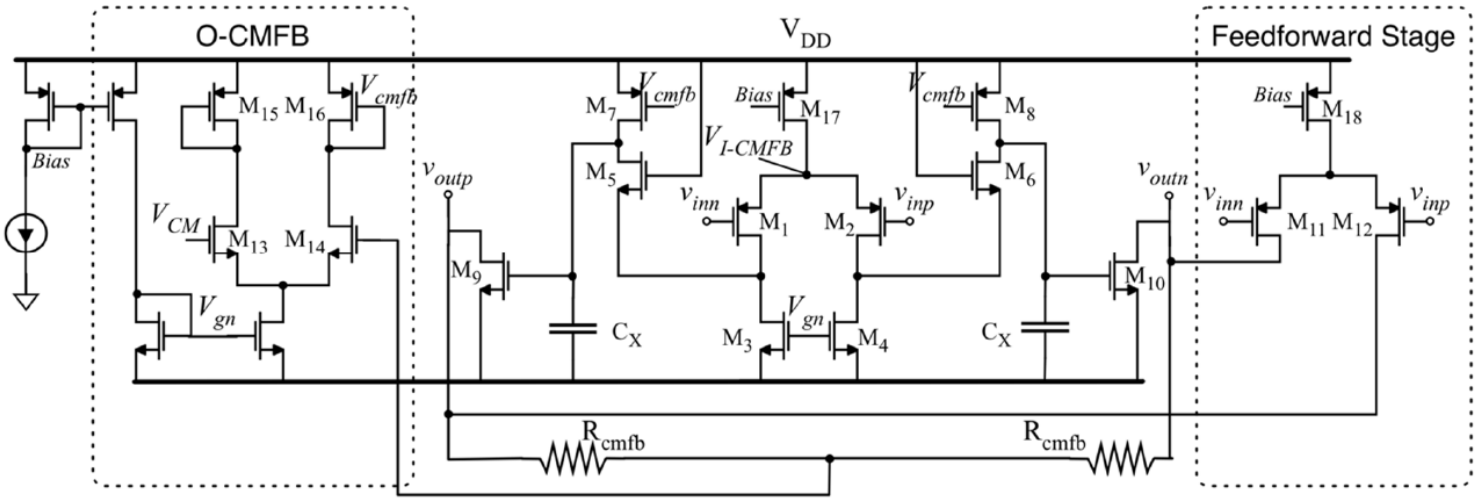

Fig. 2. Op Amp with feedforward compensation and O-CMFB circuit

CMOS 28nm process

4-bit capacitor arrays are used for frequency response programmability Filter covers the 40–105MHz range

0.7mW/pole

Area = 0.08mm^2

Stay Safe and Stay Healthy !

End of Lecture 40